#7/A
11/7/00
HAYES

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application) PATENT APPLICATION
)
Inventor(s): OM P. AGRAWAL et al.)
)
SC/Serial No.: 09/235,615) Art Unit: 2819
)
Filed: January 21, 1999) Examiner: D. Chang
)
Title: FPGA INTEGRATED CIRCUIT HAVING EMBEDDED)
SRAM MEMORY BLOCKS WITH REGISTERED)
ADDRESS AND DATA INPUT SECTIONS)

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to **Commissioner for Patents, Washington, D.C. 20231**, on October 24, 2000.

(Attorney Signature)

Gideon Gimlan, Reg. No. 31,955
Signature Date: October 24, 2000

RESPONSE [A] TO OFFICE ACTION UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

This RESPONSE [A] is in reply to the Office action mailed 07/05/00.

Amendments

Please amend the above-identified application as follows:

In the Specification,

Please amend the Specification as follows.

Page 1:

lines 15-16: Please delete "[Attorney Docket No. AMDI 8222]";

Page 2:

Attorney Docket No.: LATC-08320US0 MCF/GGG
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